Amendments to the Specification:

Please add the paragraph on page 3, after paragraph [0018] and before the title Detailed Description of the Invention:

Figure 5B illustrates a cross-sectional view orthogonal to Figure 5A and extending in the channel region.

Please replace the paragraph [0021] on page 5 with the following rewritten paragraph:

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the $10^{15}/cm^3$ to $10^{17}/cm^3$ range with the high $10^{16}/cm^3$ range being preferred. The process of the present invention begins by forming a layer of pad nitride film 16 of about 100 nm thickness and a pad oxide 12 of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

Please replace the paragraph [0025] on page 5 with the following rewritten paragraph:

Referring now to Figure 3, in the first alternative embodiment of the invention a disposable hard mask 41of, for example borosilicate glass (BSG), arsenic doped glass (ASG), other doped glass or ozone TEOS is deposited and the active area patterned as shown in Figure 3A using ~~and~~ an active area mask and etch procedure to separate transistors. This active area is generally rectangular

with the etched silicon forming an "H" or "I" shaped pattern within it. The ends form the source and drain 42 of the transistor and the central regions of each are joined by a silicon conduction channel 14. The polysilicon outside the active area is etched down to the BOX ~~14~~ 12. This etching process also removes pad nitride and monocrystalline silicon if not masked, leaving a single transistor structure, as shown, for each active area mask. However, as alluded to above, with appropriate spacing of pad nitride deposits a transistor can be formed under each pad nitride deposit. The active area masks would thus only allow separating of the gate polysilicon 20 between transistors. Even this separation of transistors may be eliminated in some applications in arrays where the gates form bit lines or word lines.

Please replace the paragraph [0027] on page 6 with the following rewritten paragraph:

Alternatively, as illustrated in Figure 3B, the disposable active area hard mask 41 is applied and patterned and etching to the BOX ~~14~~ 12 is performed as before. Then the hard mask is stripped and a conformal layer 34 of polysilicon and silicide (e.g. ~~WSiX~~ WSi_x or silicides of cobalt of titanium) is deposited, again by chemical vapor deposition. (In addition, the silicides may be replaced by a combination of tungsten and barrier tungsten nitride, tantalum nitride, tantalum silicon nitride or any other known, low-resistance material. Additional mask material such as boron or arsenic doped glass (BSG or ASG) or Ozone TEOS is applied and etched to form sidewalls 32. The silicide ~~(~~ and underlying polysilicon is then etched to the buried oxide and all remaining mask material is stripped. This process thus provides the preferred liner shape 34 of the silicide.